What is claimed is:

1. A phase multiplier subcircuit, comprising:

first and second subcircuit power supply terminals;

a PULLUPBIAS subcircuit terminal;

a COMMON subcircuit terminal;

INA and /INB subcircuit terminals;

OUTA, /OUTB, and OUTB subcircuit terminals;

a first dual-gate transistor having a single drain, a first gate coupled to the OUTB subcircuit terminal, a second gate coupled to the /INB subcircuit terminal, and a single source coupled to the COMMON subcircuit terminal;

a first transistor having a gate and a drain coupled to the single drain of the first dual-gate transistor, and a source coupled to the first subcircuit power supply terminal;

a second transistor having a drain coupled to a BIASP integration node, a gate coupled to the gate of the first transistor, and a source coupled to the first subcircuit power supply terminal;

a third transistor having a drain coupled to the BIASP node, a gate coupled to the PULLUPBIAS subcircuit terminal, and a source coupled to the second subcircuit power supply terminal;

a fourth transistor having a drain coupled to a BIASN node, a gate coupled to the BIASP node, and a source coupled to the second subcircuit power supply terminal;

a fifth transistor having a gate and a drain coupled to the BIASN node, and a source coupled to the first subcircuit power supply terminal;

a second dual-gate transistor having a single drain, a first gate coupled to the BIASP node, a second gate coupled to the INA subcircuit terminal, and a single source coupled to the second subcircuit power supply terminal;

a third dual-gate transistor having a single drain coupled to the single drain of the second dual-gate transistor, a first gate coupled to the BIASN node, a second gate coupled to the INA subcircuit terminal, and a single source coupled to the first subcircuit power supply terminal;

a fourth dual-gate transistor having a single drain coupled to the OUTA subcircuit terminal, a first gate coupled to the BIASP node, a second gate coupled to the single drain of the third dual-gate transistor, and a single source coupled to the second subcircuit power supply terminal;

a fifth dual-gate transistor having a single drain coupled to the OUTA subcircuit terminal, a first gate coupled to the BIASN node, a second gate coupled to the drain of the third dual-gate transistor, and a single source coupled to the first subcircuit power supply terminal;

a first inverter having an output terminal coupled to the /OUTB subcircuit terminal, and an input terminal coupled to the OUTA subcircuit terminal; and

a second inverter having an output terminal coupled to the OUTB subcircuit terminal, and an input terminal coupled to the /OUTB subcircuit terminal.

2. The phase multiplier subcircuit of claim **1**, wherein:

the first inverter comprises:

a sixth transistor having a drain coupled to the /OUTB subcircuit terminal, a gate coupled to the OUTA subcircuit terminal, and a source coupled to the first subcircuit power supply terminal; and

a seventh transistor having a drain coupled to the /OUTB subcircuit terminal, a gate coupled to the OUTA subcircuit terminal, and a source coupled to the second subcircuit power supply terminal; and

the second inverter comprises:

an eighth transistor having a drain coupled to the OUTB subcircuit terminal, a gate coupled to the /OUTB subcircuit terminal, and a source coupled to the first subcircuit power supply terminal; and

a ninth transistor having a drain coupled to the OUTB subcircuit terminal, a gate coupled to the /OUTB subcircuit terminal, and a source coupled to the second subcircuit power supply terminal.

3. A phase multiplier circuit comprising:

first and second power supply terminals;

an input signal terminal;

first, second, third, and fourth output terminals;

a COMMON node;

a PULLUPBIAS node;

a first inverter having an output terminal, and an input terminal coupled to the input signal terminal;

a second inverter having an output terminal coupled to the first output terminal, and an input terminal coupled to the output terminal of the first inverter;

a plurality of phase multiplier subcircuits, each comprising:

first and second subcircuit power supply terminals;

a PULLUPBIAS subcircuit terminal;

a COMMON subcircuit terminal;

INA and /INB subcircuit terminals;

OUTA, /OUTB, and OUTB subcircuit terminals;

a first dual-gate transistor having a single drain, a first gate coupled to the OUTB subcircuit terminal, a second gate coupled to the /INB subcircuit terminal, and a single source coupled to the COMMON subcircuit terminal;

a first transistor having a gate and a drain coupled to the single drain of the first dual-gate transistor, and a source coupled to the first subcircuit power supply terminal;

a second transistor having a drain coupled to a BIASP integration node, a gate coupled to the gate of the first transistor, and a source coupled to the first subcircuit power supply terminal;

a third transistor having a drain coupled to the BIASP node, a gate coupled to the PULLUPBIAS subcircuit terminal, and a source coupled to the second subcircuit power supply terminal;

a fourth transistor having a drain coupled to a BIASN node, a gate coupled to the BIASP node, and a source coupled to the second subcircuit power supply terminal;

a fifth transistor having a gate and a drain coupled to the BIASN node, and a source coupled to the first subcircuit power supply terminal;

a second dual-gate transistor having a single drain, a first gate coupled to the BIASP node, a second gate coupled to the INA subcircuit terminal, and a single source coupled to the second subcircuit power supply terminal;

a third dual-gate transistor having a single drain coupled to the single drain of the second dual-gate transistor, a first gate coupled to the BIASN node, a second gate coupled to the INA subcircuit terminal, and a single source coupled to the first subcircuit power supply terminal;

a fourth dual-gate transistor having a single drain coupled to the OUTA subcircuit terminal, a first gate coupled to the BIASP node, a second gate coupled to the single drain of the third dual-gate transistor, and a single source coupled to the second subcircuit power supply terminal;

a fifth dual-gate transistor having a single drain coupled to the OUTA subcircuit terminal, a first gate coupled to the BIASN node, a second gate coupled to the drain of the third dual-gate transistor, and a single source coupled to the first subcircuit power supply terminal;

a first inverter having an output terminal coupled to the /OUTB subcircuit terminal, and an input terminal coupled to the OUTA subcircuit terminal; and

a second inverter having an output terminal coupled to the OUTB subcircuit terminal, and an input terminal coupled to the /OUTB subcircuit terminal;

a first one of the plurality of phase multiplier subcircuits wherein:

the first subcircuit power supply terminal is coupled to the first power supply terminal;

the second subcircuit power supply terminal is coupled to the second power supply terminal;

the PULLUPBIAS subcircuit terminal is coupled to the PULLUPBIAS node;

the COMMON subcircuit terminal is coupled to the COMMON node;

the INA subcircuit terminal is coupled to the input signal terminal;

the /INB subcircuit terminal is coupled to the first inverter's output terminal; and

the OUTB subcircuit terminal is coupled to the second output terminal.

a second one of the plurality of phase multiplier subcircuits wherein:

the first subcircuit power supply terminal is coupled to the first power supply terminal;

the second subcircuit power supply terminal is coupled to the second power supply terminal;

the PULLUPBIAS subcircuit terminal is coupled to the PULLUPBIAS node;

the COMMON subcircuit terminal is coupled to the COMMON node;

the INA subcircuit terminal is coupled to the first phase multiplier subcircuit's OUTA terminal;

the /INB subcircuit terminal is coupled to the first phase multiplier subcircuit's /OUTB terminal; and

the OUTB subcircuit terminal is coupled to the third output terminal.

a third one of the plurality of phase multiplier subcircuits wherein:

the first subcircuit power supply terminal is coupled to the first power supply terminal;

the second subcircuit power supply terminal is coupled to the second power supply terminal;

the PULLUPBIAS subcircuit terminal is coupled to the PULLUPBIAS node;

the COMMON subcircuit terminal is coupled to the COMMON node;

the INA subcircuit terminal is coupled to the second phase multiplier subcircuit's OUTA terminal;

the /INB subcircuit terminal is coupled to the second phase multiplier subcircuit's /OUTB terminal; and

the OUTB subcircuit terminal is coupled to the fourth output terminal;

a sixth dual-gate transistor having a single drain coupled to a second node, a first gate coupled to the first output terminal, a second gate coupled to the third phase multiplier's /OUTB terminal, and a single source coupled to the COMMON node;

a sixth transistor having a gate and a drain coupled to the second node, and a source coupled to the first power supply terminal;

a seventh transistor having a drain coupled to the PULLUPBIAS node, a gate coupled to the gate of the sixth transistor, and a source coupled to the first power supply terminal; and

an eighth transistor having a gate and a drain coupled to the PULLUPBIAS node, and a source coupled to the second power supply terminal.

4. The phase multiplier circuit of claim 3, wherein the COMMON node is coupled to the second power supply terminal.

5. The phase multiplier circuit of claim 3, further comprising a current source coupled between the COMMON node and the second power supply terminal.

6. The phase multiplier circuit of claim 4, wherein:

the sixth dual-gate transistor, and the first dual-gate transistor of the first, second, and third phase multiplier subcircuits have substantially the same physical dimensions;

the sixth transistor, and the first transistor of the first, second, and third phase multiplier subcircuits have substantially the same physical dimensions;

the seventh transistor, and the second transistor of the first, second, and third phase multiplier subcircuits have substantially the same physical dimensions; and

the eighth transistor, and the third transistor of the first, second, and third phase multiplier subcircuits have substantially the same physical dimensions.

7. The phase multiplier circuit of claim 6, wherein the first, second, and third phase multiplier subcircuits each further comprise:

a tenth transistor, providing additional loop filter capacitance, having a gate coupled to the BIASP node, and having a drain and a source coupled to the second power supply terminal; and

an eleventh transistor having a drain coupled to the BIASP node, a gate coupled to a RESET subcircuit terminal, and a source coupled to the first subcircuit power supply terminal.

8. The phase multiplier circuit of claim 7, wherein:

the RESET subcircuit terminals of the first, second, and third phase multiplier subcircuits are coupled to a RESET input terminal;

the phase multiplier circuit is at an initial state when the RESET terminal is at a logic high level; and

the phase multiplier circuit transitions from the initial state to a final state after the RESET terminal is de-asserted from a logic high level to a logic low level.

9. The phase multiplier circuit of claim 7, further comprising:

an input signal coupled to the input signal terminal;

a first power supply voltage applied to the first power supply terminal;

a second power supply voltage applied to the second power supply terminal; and

a reset signal, applied to the RESET terminal, which is asserted and then de-asserted.

10. The phase multiplier circuit of claim 9, wherein after transitioning to the final state:

the first output terminal exhibits a signal having a first phase;

the second output terminal exhibits a signal having a second phase;

the third output terminal exhibits a signal having a third phase;

the fourth output terminal exhibits a signal having a fourth phase; and

the first, second, third, and fourth phases are substantially evenly spaced between 0 and 360 degrees.

11. The phase multiplier circuit of claim **2**, wherein:

the first inverter comprises:

a tenth transistor having a drain coupled to the first phase multiplier subcircuit's /INB subcircuit terminal, a gate coupled to the input signal terminal, and a source coupled to the first power supply terminal; and

an eleventh transistor having a drain coupled to the first phase multiplier subcircuit's /INB subcircuit terminal, a gate coupled to the input signal terminal, and a source coupled to the second power supply terminal; and

the second inverter comprises:

a twelfth transistor having a drain coupled to the first output terminal, a gate coupled to the first phase multiplier subcircuit's /INB subcircuit terminal, and a source coupled to the first power supply terminal; and

a thirteenth transistor having a drain coupled to the first output terminal, a gate coupled to the first phase multiplier subcircuit's /INB subcircuit terminal, and a source coupled to the second power supply terminal.

12. A phase multiplier which generates output signals, each output signal having a phase relative to one of the output signals, said phase multiplier comprising:

means for generating substantially equal bias currents, the bias currents being proportional to a difference in phase between the output signal with the smallest phase and the output signal with the largest phase;

for each output signal except the output signal with the largest phase, means for generating a phase current proportional to a difference between the phase of the output signal and the phase of the output signal with the next-largest phase, and of a polarity opposite that of the bias currents;

for each output signal, means for generating a voltage by integrating the phase current and one of the bias currents onto a loop filter capacitance; and

means for controlling the phases which includes voltage-controlled delay elements and the generated voltages.

13. The phase multiplier of claim **12**, wherein the phases of the output signals are substantially evenly spaced between 0 and 360 degrees.

14. A phase multiplier which generates output signals, each output signal having a phase relative to one of the output signals, said phase multiplier

a bias current generator which generates a plurality of substantially equal bias currents, said plurality of bias currents being proportional to a difference in phase between the output signal with the smallest phase and the output signal with the largest phase;

a phase current generator generating a phase current for each output signal except the output signal with the largest phase, said phase currents being proportional to a

difference between the phase of the output signal and the phase of the output signal with the next-largest phase, and of a polarity opposite that of the bias currents;

a voltage generator which generates for each output signal a voltage by integrating the phase current and one of the bias currents onto a loop filter capacitance; and

a phase controller for controlling the phases.